WHAT IS CLAIMED IS:

1. A digital signal processing circuit module comprising:

an isochronous data processing circuit having at least two inputs and a data output, the isochronous circuit having a uniform processing delay to determine the data output for all valid input combinations;

a delay circuit receiving a control signal and producing a delayed control signal, the delayed control signal being produced by delaying the control signal by a time period that is substantially equal to the uniform processing delay of the data processing circuit; and

an output latch coupled to the data processing circuit and the delay circuit, the output latch latching the data output of the data processing circuit based on the delayed control signal produced by the delay circuit.

2. The digital signal processing circuit module as defined in claim 1, wherein the isochronous circuit and the delay circuit are fabricated on a single semiconductor substrate.

3. The digital signal processing circuit module as defined in claim 1,

wherein the data processing circuit includes a transistor array having two multiple line data inputs and one multiple line data output,

the delay circuit includes a transistor block having one input and one output;

the transistor array of the data processing circuit has a first number of transistors in parallel with each line of the data inputs and a second number of transistors in parallel with each line of the data output, and

the delay circuit has the first number of transistors in parallel with the input of the delay circuit and the second number of transistors in parallel with the output of the delay circuit.

4. The digital signal processing circuit module as defined in claim 1, wherein the delayed control signal produced by the delay circuit has additional output loading so as to provide an additional delay.

5. The digital signal processing circuit module as defined in claim 1, wherein the data processing circuit is one of an OHRNS adder, an OHRNS subtractor, and an OHRNS multiplier.

6. A OHRNS arithmetic processing module comprising:

an OHRNS arithmetic processing transistor array having at least one multiple line data input and at least one multiple line data output;

a delay circuit receiving a control signal at input and producing a delayed control signal at output, the delay circuit having an equal number of transistors in parallel with the input of the delay circuit as are in parallel with one of the lines of the multiple line data input of the OHRNS arithmetic processing transistor array, the delay circuit also having an equal number of transistors in parallel with the output of the delay circuit as are in parallel with one of the lines of the multiple line data output of the OHRNS arithmetic processing transistor array; and

an output latch coupled to the OHRNS arithmetic processing transistor array and the delay circuit, the output latch latching the multiple line data output of the OHRNS arithmetic processing transistor array based on the delayed control signal produced by the delay circuit.

7. The OHRNS arithmetic processing module as defined in claim 6, wherein the OHRNS arithmetic processing transistor array and the delay circuit are fabricated on a single semiconductor substrate.

8. The OHRNS arithmetic processing module as defined in claim 6, wherein the output of the delay circuit has additional output loading so as to cause an additional delay.

9. The OHRNS arithmetic processing module as defined in claim 6, wherein the OHRNS arithmetic processing transistor array is a core of one of an OHRNS adder, an OHRNS subtractor, and an OHRNS multiplier.

10. An asynchronous system comprising:

a plurality of digital signal processing circuit modules, each of the digital signal processing circuit modules having at least one data input, at least one data output, a control input, and a control output; and

a plurality of control units, each of the control units being coupled to the control output of one of the digital signal processing circuit modules,

wherein at least one of the digital signal processing circuit modules includes:

an isochronous data processing circuit coupled to the data input of the digital signal processing circuit module, the isochronous circuit having a uniform processing delay to determine the data output for all valid data inputs;

a delay circuit coupled to the control input of the digital signal processing circuit module, the delay circuit producing a delayed control signal by delaying by a time period that is substantially equal to the uniform processing delay of the data processing circuit; and

an output latch coupled to an output of the data processing circuit and to the delay circuit, the output latch latching the output of the data processing circuit based on the delayed control signal produced by the delay circuit.

11. The asynchronous system as defined in claim 10, wherein the asynchronous system is fabricated on a single semiconductor substrate.

12. The asynchronous system as defined in claim 10, wherein in the at least one of the digital signal processing circuit modules:

the data processing circuit includes a transistor array having two multiple line data inputs and one multiple line data output,

the delay circuit includes a transistor block having one input and one output;

the transistor array of the data processing circuit has a first number of transistors in parallel with each line of the data inputs and a second number of transistors in parallel with each line of the data output, and

the delay circuit has the first number of transistors in parallel with the input of the delay circuit and the second number of transistors in parallel with the output of the delay circuit.

13. The asynchronous system as defined in claim 10, wherein the data processing circuit of the at least one of the digital signal processing circuit modules is one of an OHRNS adder, an OHRNS subtractor, and an OHRNS multiplier.

14. The asynchronous system as defined in claim 10,

wherein a first of the control units has an input coupled to the control output of a first of the digital signal processing circuit modules and an output coupled to the control input of a second of the digital signal processing circuit modules, and

a second of the control units has an input coupled to the control output of the second digital signal processing circuit module and an output coupled to the control input of a third of the digital signal processing circuit modules.

15. The asynchronous system as defined in claim 14, wherein the first control unit has another input coupled to the output of the second control unit.

16. A self-timed OHRNS processing circuit comprising:

a first processing module producing a data output and an Ack output, the Ack output being toggled when the data output of the first processing module is ready;

a second processing module coupled to the first processing module, the second processing module including a Req input, an Ack output, a transistor array, and a delay circuit, the Req input of the second processing module being coupled to the Ack output of the first processing module, the Ack output of the second processing module being toggled when the data output of the second processing module is ready, the transistor array having a uniform processing delay for producing the data output for all valid inputs, and the delay circuit delaying the Req input of the second processing module by a time period that is substantially equal to the uniform processing delay of the transistor array;

a third processing module coupled to the second processing module, the third processing module including a Req input that is coupled to the Ack output of the second processing module; and

a control unit coupled between the Ack output of the first processing module and the Req input of the second processing module, the control unit controlling the timing of the toggling of the Req input of the second processing module based at least partially on the Ack output of the first processing module.

17. The self-timed OHRNS processing circuit as defined in claim 16, wherein the first, second, and third processing modules are fabricated on a single semiconductor substrate.

18. The self-timed OHRNS processing circuit as defined in claim 16, wherein the output of the delay circuit of the second processing module has additional output loading so as to cause an additional delay.

19. The self-timed OHRNS processing circuit as defined in claim 16, wherein the first, second, and third processing modules are each one of an OHRNS adder, an OHRNS subtractor, and an OHRNS multiplier.

20. The self-timed OHRNS processing circuit as defined in claim 16, wherein the control unit has another input coupled to an output of a second control unit, the second control unit having an input coupled to an Ack output of the third processing module.